PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: William Radke and Atif

Sarwari

Attorney Docket No.: 500988.02

Patent No. : US 6,956,577 B2

Serial No.

: 10/813,184

Issue Date: October 18, 2005

Filed

: March 29, 2004

Title

: EMBEDDED MEMORY SYSTEM AND METHOD INCLUDING DATA ERROR

CORRECTION

REQUEST FOR CERTIFICATE OF CORRECTION

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

A Certificate of Correction under 35 U.S.C. § 254 is respectfully requested for the above-identified patent in order to correct Patent and Trademark Office errors made during the printing of the patent. The changes in the patent needed to correct the errors are as follows:

Column, Line	Reads	Should Read	
Column 2, Line 14	"space on an graphics"	space on a graphics	
Column 3, Line 62	"operator or an"	operator of an	
Column 4, Line 33	"a bus interface-200"	a bus interface 200	
Column 4, Line 35	"optionally high-speed"	optionally to high-speed	CET 1 0 2008

Column 5, Line 3	"is portion"	is a portion
Column 5, Lines 15-	"techniques well-known"	techniques well known
Column 6, Line 54	"portion of the of the original"	portion of the original
Column 7, Line 4	"with requested data"	with the requested data
Column 8, Line 13	"CAM 350 divided into"	CAM 350 is divided into
Column 8, Line 18	"such as, whether the"	such as whether
Column 9, Line 13	"according the to"	according to the
Column 9, Line 45	"memory address:"	memory address;
Column 10, Line 45	"combined updated first data"	combined first data
Column 10, Line 65	"(EGG) generator"	(ECC) generator
Column 10, Line 67	"EGG"	ECC
Column 11, Lines 3, 4, 5, 13, 16, 21 and 34	"EGG"	ECC
Column 12, Line 4	"a second memory an output coupled to the EGC generator"	a second memory output coupled to the ECC generator
Column 12, Lines 5, 14 and 24	"EGG"	ECC

The above errors for which correction is requested under 35 U.S.C. § 254 were made in the printing of the patent or in the original application. The errors are considered sufficiently important to justify the processing of a Certificate of Correction under 35 U.S.C. § 254. A Form PTO-1050, in duplicate, is enclosed herewith.

The Commissioner is hereby authorized to charge payment of any fees associated with this communication to Deposit Account No. 50-1266. A duplicate copy of this sheet is enclosed.

Favorable consideration of this Request is respectfully requested.

Respectfully submitted,

Date: Sept. 26, 2006

By: Edward W. Bulchis, Reg. No. 26,847

Customer No. 27,076
Dorsey & Whitney LLP
1420 Fifth Avenue, Suite 3400
Seattle, WA 98101
(206) 903-8785
Attorney for Applicant(s)

EWB:tdp

Enclosures:

Postcard

Form PTO-1050 (+ copy)

h:\ip\clients\rendition\500988.02\500988.02 req cert correct.doc

UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO.

US 6,956,577 B2

DATED

October 18, 2005

INVENTOR(S)

William Radke and Atif Sarwari

It is certified that errors appear in the above identified patent and that said Letters Patent is hereby corrected as shown below:

Column, Line	Reads	Should Read
Column 2, Line 14	"space on an graphics"	space on a graphics
Column 3, Line 62	"operator or an"	operator of an
Column 4, Line 33	"a bus interface-200"	a bus interface 200
Column 4, Line 35	"optionally high-speed"	optionally to high-
Column 5, Line 3	"is portion"	speedis a portion
•	•	is a portion
Column 5, Lines 15-16	"techniques well-known"	techniques well known
Column 6, Line 54	"portion of the of the original"	portion of the original
Column 7, Line 4	"with requested data"	with the requested data
Column 8, Line 13	"CAM 350 divided into"	CAM 350 is divided
		into
Column 8, Line 18	"such as, whether the"	such as whether
Column 9, Line 13	"according the to"	according to the
Column 9, Line 45	"memory address:"	memory address;
Column 10, Line 45	"combined updated first data"	combined first data
Column 10, Line 65	"(EGG) generator"	(ECC) generator
Column 10, Line 67	"EGG"	ECC
Column 11, Lines 3, 4, 5,	"EGG"	ECC
13, 16, 21 and 34		
Column 12, Line 4	"a second memory an	a second memory output

	output coupled to the EGC generator"	coupled to the ECC generator
Column 12, Lines 5, 14 and 24	"EGG"	ECC

MAILING ADDRESS OF SENDER:

Patent No. <u>US 6,956,577 B2</u>

DORSEY & WHITNEY LLP 1420 Fifth Avenue, Suite 3400 Seattle, Washington 98101

No. add'l. copies @ .30 per page

FORM PTO-1050 (REV. 3-82)

h:\ip\clients\rendition\500988.02\500988.02 pto 1050.doc

PATENT

I hereby certify that the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: William Radke and Atif

Attorney Docket No.: 500988.02

Sarwari

Patent No. : US 6,956,577 B2

Serial No.

: 10/813,184

Issue Date: October 18, 2005

Filed

: March 29, 2004

Title

: EMBEDDED MEMORY SYSTEM AND METHOD INCLUDING DATA ERROR

CORRECTION

REQUEST FOR CERTIFICATE OF CORRECTION

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

A Certificate of Correction under 35 U.S.C. § 254 is respectfully requested for the above-identified patent in order to correct Patent and Trademark Office errors made during the printing of the patent. The changes in the patent needed to correct the errors are as follows:

Column, Line	Reads	Should Read
Column 2, Line 14	"space on an graphics"	space on a graphics
Column 3, Line 62	"operator or an"	operator of an
Column 4, Line 33	"a bus interface-200"	a bus interface 200
Column 4, Line 35	"optionally high-speed"	optionally to high-speed-

Column 5, Line 3	"is portion"	is a portion
Column 5, Lines 15-	"techniques well-known"	techniques well known
Column 6, Line 54	"portion of the of the original"	portion of the original
Column 7, Line 4	"with requested data"	with the requested data
Column 8, Line 13	"CAM 350 divided into"	CAM 350 is divided into
Column 8, Line 18	"such as, whether the"	such as whether
Column 9, Line 13	"according the to"	according to the
Column 9, Line 45	"memory address:"	memory address;
Column 10, Line 45	"combined updated first data"	combined first data
Column 10, Line 65	"(EGG) generator"	(ECC) generator
Column 10, Line 67	"EGG"	ECC
Column 11, Lines 3, 4, 5, 13, 16, 21 and 34	"EGG"	ECC
Column 12, Line 4	"a second memory an output	a second memory output coupled
	coupled to the EGC generator"	to the ECC generator
Column 12, Lines 5, 14 and 24	"EGG"	ECC

The above errors for which correction is requested under 35 U.S.C. § 254 were made in the printing of the patent or in the original application. The errors are considered sufficiently important to justify the processing of a Certificate of Correction under 35 U.S.C. § 254. A Form PTO-1050, in duplicate, is enclosed herewith.

The Commissioner is hereby authorized to charge payment of any fees associated with this communication to Deposit Account No. 50-1266. A duplicate copy of this sheet is enclosed.

Favorable consideration of this Request is respectfully requested.

Respectfully submitted,

Date: Sept. 26, 2006

By: Edward W. Bulchis, Reg. No. 26,847

Customer No. 27,076
Dorsey & Whitney LLP
1420 Fifth Avenue, Suite 3400
Seattle, WA 98101
(206) 903-8785
Attorney for Applicant(s)

EWB:tdp

Enclosures:

Postcard

Form PTO-1050 (+ copy)

 $h:\linction \verb|\500988.02| 500988.02 req cert correct.doc|$

UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO.

US 6,956,577 B2

DATED

October 18, 2005

INVENTOR(S)

William Radke and Atif Sarwari

It is certified that errors appear in the above identified patent and that said Letters Patent is hereby corrected as shown below:

Column, Line	Reads	Should Read
Column 2, Line 14	"space on an graphics"	space on a graphics
Column 3, Line 62	"operator or an"	operator of an
Column 4, Line 33	"a bus interface-200"	a bus interface 200
Column 4, Line 35	"optionally high-speed"	optionally to high- speed
Column 5, Line 3	"is portion"	is a portion
Column 5, Lines 15-16	"techniques well-known"	techniques well known
Column 6, Line 54	"portion of the of the original"	portion of the original
Column 7, Line 4	"with requested data"	with the requested data
Column 8, Line 13	"CAM 350 divided into"	CAM 350 is divided
·		into
Column 8, Line 18	"such as, whether the"	such as whether
Column 9, Line 13	"according the to"	according to the
Column 9, Line 45	"memory address:"	memory address;
Column 10, Line 45	"combined updated first data"	combined first data
Column 10, Line 65	"(EGG) generator"	(ECC) generator
Column 10, Line 67	"EGG"	ECC
Column 11, Lines 3, 4, 5, 13, 16, 21 and 34	"EGG"	ECC
Column 12, Line 4	"a second memory an	a second memory output

	output coupled to the EGC generator"	coupled to the ECC generator
Column 12, Lines 5, 14 and 24	"EGG"	ECC
	*	

MAILING ADDRESS OF SENDER:

DORSEY & WHITNEY LLP 1420 Fifth Avenue, Suite 3400 Seattle, Washington 98101

FORM PTO-1050 (REV. 3-82)

 $h:\lip\clients\clien$

Patent No. <u>US 6,956,577 B2</u>

No. add'l. copies

@ .30 per page